REMARKS

The last Office Action, which has been made final, and the references cited by the Examiner have been carefully considered. The claims have been amended in a sincere effort to define more clearly and more specifically features of Applicant's invention which distinguish over the art of record.

In the last Office Action, Claims 1-5 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,708,284 (Onishi). With respect to Claims 1-4, the Examiner contends that the Onishi patent discloses a non-volatile random access memory having an insulation film 7 with a concave portion at a top surface, a laminated body obtained by laminating a plurality of layers on the top surface and etching a region of the plurality of layers corresponding to a region other than the concave portion, where the laminated body includes a lower electrode 8 which is brought into contact with a bottom surface of the concave portion, a ferroelectric layer 9 formed on the lower electrode 8, and an upper electrode layer 10 formed on the ferroelectric layer 9. The Examiner further contends that the laminated body disclosed in the Onishi patent includes a portion of the lower electrode layer 8 protruding outwardly from an inner peripheral edge forming the concave portion 8, and a side of the portion of the lower electrode 8, a side of the ferroelectric layer 9 and a side of the upper electrode layer 10 are flush with each other. In this regard, the Examiner refers to Figure 6 of the Onishi patent. The Examiner further contends that the Onishi patent discloses a film 8a formed in a bottom of the hollow and separating between the insulation film 7 and the lower electrode layer 8b, and refers to Figure 6 of the Onishi patent for disclosing this, and that the lower electrode 8 includes a first electrode portion 8a formed at the corner of the hollow and a second electrode portion 8b formed on the first electrode portion 8a, again

Claim 5 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of the Onishi patent and newly cited U.S. Patent No. 5,767,541 (Hanagasaki). The Examiner acknowledges that the Onishi patent does not disclose the top surfaces of the lower electrode and the insulating film being planarized flush with each other. However, the Examiner contends that the Hanagasaki patent discloses the lower electrode 8 being planarized flush with the insulating film, and refers to Figure 1e of the Hanagasaki patent. The Examiner withdrew the Aoki et al. patent as a reference against Claims 1-5.

The rejection of Claims 1-5 in view of the Onishi patent, and the rejection of Claim 5 in view of the combination of the Onishi patent and the Hanagasaki patent, especially in view of the changes made to Claims 2 and 3 herein, are respectfully traversed. Addressing Claim 2 and the amendments made therein first, the new limitations placed in Claim 2 are made to emphasize that the additional film which is embedded from the top surface of the insulation film in a position of a predetermined depth is exposed only at a bottom of the hollow. As shown in Figure 9 of the drawings of the subject application, film 38, which may be formed of silicon nitride (Sin), silicon nitride oxide (SiON) or the like is used as an etch stop for forming the hollow 14. It is only exposed at the bottom of the hollow 14. It is not exposed anywhere else on the ferroelectric memory. This structural limitation is emphasized by adding the word "only" to Claim 2. Film 38 allows the hollow 24 to be formed at a predetermined depth in the first insulation film 12, and the top surface of the upper electrode 20 may be made flat, as shown in Figure 9 of the subject application.

In contrast, and as shown in Figure 6 of the Onishi patent, the Onishi patent does not disclose an insulating film at a predetermined depth in the insulating layer 7 to separate the insulating layer 7 from the lower electrode 8 in the contact hole 4. More specifically, in the Onishi patent, reference numeral 8a refers to a TiN/Ti film, which is a conductor film. This

so it cannot be equivalent to the film 38 which is specifically defined by amended Claim 2 as being an etch stop for forming the hollow to a predetermined depth.

Furthermore, film 8a formed of TiN/Ti is not exposed only at the bottom of the contact hole 4, as specifically called for in amended Claim 2, but it also is exposed at the side of the hole, as shown in Figure 6 of the Onishi patent.

In the claimed invention, by including insulating film 38, which is exposed only at the bottom of the hole 14, film 38 functions as an etch stop layer, and the upper surface of the lower electrode 16 can be made flat. The result is a ferroelectric memory which is highly integrated. The Onishi patent does not disclose such structure.

Now addressing amended Claim 3, this claim has been particularly amended to add the word "only" to emphasize that the first electrode portion of the lower electrode layer is formed only at a corner of the hollow. Reference is respectfully made to Figure 10 of the drawings, where it is shown that the first electrode portion 16a is formed only at the corner of the hollow 14. The second electrode portion 16b can then be formed in the hollow to provide the lower electrode 16. The advantage of this structure is that the top surface of the upper electrode 20 may be maintained in a flat state, as shown in Figure 10 of the drawings. As specifically stated in the specification, at page 10, lines 6-19 thereof, with first and second electrode portions 16a, 16b formed in the hollow, and with second electrode portion 16b being formed by a spin coat process, the amount of depression which may result in the center of the top surface of the second electrode portion 16b may be decreased when the lower electrode 16 is baked. Also, if the second electrode portion 16b or the first conductive film 26b is formed by sputtering, the variation in the crystalline orientation may be reduced in the top surface of the lower electrode 16. This latter embodiment is shown in Figure 11 of the subject application. This serves to stabilize the crystalline state of the ferroelectric 18 which

Such structure is not disclosed in the Onishi patent. In particular, and as shown in Figure 6 of the Onishi patent, the lower electrode 8 is formed of the TiN/Ti film 8a and the Pt film 8b. It is clear that the TiN/Ti film is formed not only over the entire bottom of the contact hole 4 but also at the side of the hole, because the TiN/Ti film acts as the barrier metal. Accordingly, the structure of the random access memory disclosed in the Onishi patent differs from that now more particularly and specifically set forth in amended Claim 3.

Turning now to Claim 4, the structure set forth in Claim 4 is shown, by example, in Figure 8. Claim 4 specifically calls for a ferroelectric memory having an insulation film with a concave portion, and a laminated body having a lower electrode layer which is brought into contact with a bottom surface of the concave portion, a thin film of the same material as that of the lower electrode layer formed on the surface of the lower electrode layer, a ferroelectric layer formed on the thin film and an upper electrode layer formed on the ferroelectric layer, and further wherein a side of the thin film, the ferroelectric layer and the upper electrode layer are flush with each other. As shown in Figure 8, the thin film 36 is made from the same material as the first conductive film, i.e., lower electrode 26. The thin film 36 is formed on the planarized first conductive film 26. The advantage of having a thin film 36 formed on the surface of the planarized first conductive film 26 and using for the thin film 36 the same material as the first conductive film 26 is that it eliminates the surface roughening in the first conductive film which is caused by the planarization process. This is disclosed at page 9, lines 17-20 of the subject application.

The Onishi patent discloses structure which is different from that set forth in Claim 4 of the pending application. As shown in Figure 6 of the Onishi patent, no layer made of the same material (Pt) as the lower electrode is formed between the lower electrode 8 and the ferroelectric film 9. Accordingly, this "same material" limitation found in Claim 4 of the

Turning to Claim 1 now, the ferroelectric memory of the subject application is defined in Claim 1 as having a lower electrode layer wherein a portion of only the lower electrode layer is embedded in the concave portion and protrudes outwardly from the inner peripheral edge of the insulation film which forms the concave portion. Because of this, the top surface of the upper electrode 20 may be made flat. This allows the ferroelectric memory and its constituent laminated layers to be highly integrated. It is emphasized that Claim 1 specifies that only a portion of the lower electrode layer, the side surface of the ferroelectric layer, and the side surface of the upper electrode layer are flushed with each other. In contrast, the Onishi Patent discloses a random access memory in which, as shown in Figure 6, the entire or whole side surface of the lower electrode 8 is made flush with the side surface of the ferroelectric layer 9. Accordingly, this structure differs from that specifically set forth in Claim 1 of the subject application.

Claim 5 of the subject application has been rejected as being obvious in view of the combination of the Onishi patent and the newly cited Hanagasaki patent. Claim 5 defines the ferroelectric memory of the present invention as having an insulation film having a concave portion, and a laminated body having a lower electrode layer, a ferroelectric layer formed on the lower electrode layer and an upper electrode layer formed on the ferroelectric layer. The claim specifically defines the lower electrode layer and the insulation film at their respective top surfaces as being planarized flush with each other, and further defines a side of the ferroelectric layer and the side of the upper electrode layer as being flush with each other.

Figure 7 of the drawings of the subject application shows an example of the structure which is defined by Claim 5. As shown in Figure 7, the top surfaces of the first conductive film (i.e., the lower electrode) 26 and the insulation film 12 are planarized flush with each other. Because of this, the etch time can be even further shortened, because there is no need

The Examiner acknowledges that the Onishi patent does not disclose that the top surfaces of the lower electrode and the insulating film are planarized flush with each other. He cites, however, the Hanagasaki patent as disclosing, in Figure 1e, that thc lower electrode is planarized flush with the insulating film. However, the lower electrode is not the W plug 8 which is shown in Figure 1e to residc in insulating film 7, but rather is the lower electrode 9a shown in Figure 1g of the Hanagasaki patent. The specification of the Hanagasaki patent, in particular, at Col. 7, line 30, refers to the W plug as being reference numeral 8. The lowcr electrode 9a shown in Figure 1g of the Hanagasaki patent is clearly shown as not having its top surface planarized flush with the top surface of insulating film 7. In fact, electrode 9a rests above and on top of the top surface of insulating film 7, as clearly shown in Figure 1g of the Hanagasaki patent.

Accordingly, it is respectfully urged that the Hanagasaki patent, alone or in combination, does not teach or suggest that the top surface of the lower electrode and the top surface of the insulating film are flush with each other. Nor is the structures of the Onishi and Hanagasaki patents combinable, in the sense that they are completely different from one another and, even if theoretically combined, they would not make a ferroelectric memory where the top surface of the lower electrode would be flush with the top surface of the insulating layer.

Accordingly, it is respectfully urged that Claims 1-5 patentably distinguish over the refcrences of record and are allowable.

In view of the foregoing amendments and remarks, entry of the amendments to Claims 2 and 3 and favorable consideration of Claims 2 and 3, reconsideration of Claims 1, 4 and 5 and allowance of the application with Claims 1-5 are respectfully solicited. No new matter has been added by the amendments to Claims 2 and 3 herein, and no further search of the prior art is required by the amendments made herein. The amendments herein are made to place this application in better form for appeal or allowance.

Respectfully submitted,

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VERSION OF AMENDMENT WITH MARKS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend Claims 2 and 3 by rewriting the same as follows:

2. (Thrice Amended) A ferroelectric memory, comprising:

an insulation film having a hollow at a top surface; and

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said hollow, wherein said laminated body includes a lower electrode layer, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer; and the memory further comprising another film embedded from said top surface of said insulation film in a position of a predetermined depth, exposed only at a bottom of said hollow and separating between said insulation film and said lower electrode layer in said hollow, said another film being an etch stop for forming the hollow to said predetermined depth.

3. (Thrice Amended) A ferroelectric memory, comprising:

an insulation film having a hollow at a top surface; and

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said hollow, wherein said laminated body includes a lower electrode layer, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer, and said lower electrode layer includes a first electrode portion formed only at a corner of said hollow and a second portion formed on said first electrode portion.